

CLAIMS

What is claimed is:

Claim 1. A semiconductor structure formed on a substrate comprising:

a plurality of field effect transistors having a first portion of field effect transistors (FETS) and a second portion of field effect transistors;

a first stress layer having a first thickness and being configured to impart a first determined stress to the first portion of the plurality of field effect transistors; and

a second stress layer having a second thickness and being configured to impart a second determined stress to the second portion of the plurality of field effect transistors.

Claim 2. The semiconductor structure according to claim 1, wherein:

the first portion of the plurality of field effect transistors have spacings between adjacent field effect transistors that fall within a first defined spacing range; and

the second portion of the plurality of field effect transistors have spacings between adjacent field effect transistors that fall within a second defined spacing range.

Claim 3. The semiconductor structure according to claim 2, wherein:

the first defined spacing range is less than the second defined spacing range; and

the first thickness is less than the second thickness.

Claim 4. The semiconductor structure according to claim 3, wherein the first thickness does not pose a substantial risk of void formation in the first stress layer.

Claim 5. The semiconductor structure according to claim 2, wherein:

the first determined stress enhances performance of the first portion of the plurality of field effect transistors, without materially degrading performance of any of the plurality of FETs that are not in the first portion; and

the second determined stress enhances performance of the second portion of the plurality of field effect transistors, without materially degrading performance of any of the plurality of FETs that are not in the second portion.

Claim 6. The semiconductor structure according to claim 5, wherein:

the first portion of the plurality of field effect transistors is comprised of n-channel field effect transistors;

the first determined stress is a tensile stress;

the second portion of the plurality of field effect transistors is comprised of p-channel field effect transistors; and

the second determined stress is a compressive stress.

Claim 7. The semiconductor structure according to claim 6, wherein:

the first stress layer is formed by a chemical vapor deposition process using a temperature of about 480° C, a pressure of about 6.25 Torr, a spacing between the

semiconductor structure and CVD electrode of about 490 mils, a flow of about 300 sccm of 2% dilute SiH_4 gas, about 15 sccm NH_3 gas and about 1060 sccm N_2 gas using RF power of about 340 watts.

Claim 8. The semiconductor structure according to claim 6, wherein:

the second stress layer is formed by a chemical vapor deposition process using a temperature of about 480° , a pressure of about 5.75 Torr, a spacing between the semiconductor structure and CVD electrode of about 395 mils, a flow of about 3000 sccm of 2% dilute SiH_4 gas, about 15 sccm of NH_3 gas and 1060 sccm of N_2 gas using RF power of 900 watts.

Claim 9. The semiconductor structure according to claim 5, wherein:

the first portion of the plurality of field effect transistors is comprised of n-channel field effect transistors;

the first determined stress is a tensile stress;

the first defined spacing range is less than the second defined spacing range; and

the second portion of the plurality of field effect transistors is comprised of n-channel field effect transistors;

the second determined stress is a tensile stress;

the first thickness is less than the second thickness; and

the first thickness does not pose a substantial risk of void formation in the first stress layer.

Claim 10. The semiconductor structure according to claim 5, wherein:

- the first portion of the plurality of field effect transistors is comprised of p-channel field effect transistors;

- the first determined stress is a compressive stress;

- the first defined spacing range is less than the second defined spacing range; and

- the second portion of the plurality of field effect transistors is comprised of p-channel field effect transistors;

- the second determined stress is a compressive stress;

- the first thickness is less than the second thickness; and

- the first thickness does not pose a substantial risk of void formation in the first stress layer.

Claim 11. A semiconductor structure formed on a substrate comprising:

- a first plurality of n-channel field effect transistors having spacings between adjacent n-channel field effect transistors that fall within a first defined spacing range;

- a second plurality of n-channel field effect transistors having spacings between adjacent n-channel field effect transistors that fall within a second defined spacing range;

- a first plurality of p-channel field effect transistors having spacings between adjacent p-channel field effect transistors that fall within a third defined spacing range;

- a second plurality of p-channel field effect transistors having spacings between adjacent p-channel field effect transistors that fall within a fourth defined spacing range;

a first tensile layer having a first tensile layer thickness and being configured to impart a first determined tensile stress to the first plurality of n-channel field effect transistors;

a second tensile layer having a second tensile layer thickness and being configured to impart a second determined tensile stress to the second plurality of n-channel field effect transistors;

a first compressive layer having a first compressive layer thickness and being configured to impart a first determined compressive stress to the first plurality of p-channel field effect transistors; and

a second compressive layer having a second compressive layer thickness and being configured to impart a second determined compressive stress to the second plurality of p-channel field effect transistors.

Claim 12. The semiconductor structure according to claim 11, wherein each of the first tensile layer; second tensile layer; first compressive layer and second compressive layer is deposited on an SiO₂ liner.

Claim 13. The semiconductor structure according to claim 11, wherein:

the first defined spacing range is less than the second defined spacing range; and
the third defined spacing range is less than the fourth defined spacing range.

Claim 14. The semiconductor structure according to claim 13, wherein:

the first tensile layer thickness is less than the second tensile layer thickness; and
the first compressive layer thickness is less than the second compressive layer thickness.

Claim 15. The semiconductor structure according to claim 14, wherein:

the first tensile layer thickness does not pose a substantial risk of void formation in the first tensile layer; and

the first compressive layer thickness does not pose a substantial risk of void formation in the first compressive layer.

Claim 16. The semiconductor structure according to claim 15, wherein:

the first determined tensile stress enhances electron mobility in the first plurality of n-channel field effect transistors, without materially degrading performance of the first plurality of p-channel field effect transistors and the second plurality of p-channel field effect transistors; and

the first determined compressive stress enhances hole mobility in the first plurality of p-channel field effect transistors, without materially degrading performance of the first plurality of n-channel field effect transistors and the second plurality of n-channel field effect transistors.

Claim 17. The semiconductor structure according to claim 16, wherein:

the first tensile layer thickness is proportional to the first determined spacing

range;

the second tensile layer thickness is proportional to the second determined spacing range;

the first compressive layer thickness is proportional to the third determined spacing range; and

the second compressive layer thickness is proportional to the fourth determined spacing range.

Claim 18. The semiconductor structure according to claim 16, wherein the first tensile layer, second tensile layer, first compressive layer and second compressive layer, are comprised of materials from the group consisting of silicon nitride and silicon oxynitride.

Claim 19. The semiconductor structure according to claim 16, wherein:

the first tensile layer and second tensile layer each exhibit a tensile stress of about 600 to 1500 MPa; and

the first compressive layer and second compressive layer each exhibit a compressive stress of about -600 to -1500 MPa.

Claim 20. A process of forming a semiconductor structure, comprising:

forming a plurality of field effect transistors on a semiconductor substrate, the plurality of field effect transistors including a first portion of field effect transistors and a second portion of field effect transistors;

depositing a first stress layer having a first thickness and being configured to impart a first determined stress to the first portion of the plurality of field effect transistors; and

depositing a second stress layer having a second thickness and being configured to impart a second determined stress to the second portion of the plurality of field effect transistors.

Claim 21. A process of forming a semiconductor structure according to claim 20, further comprising:

removing portions of the first stress layer from areas of the semiconductor that would not experience performance enhancement due to the first determined stress; and

removing portions of the second stress layer from areas of the semiconductor that would not experience performance enhancement due to the second determined stress.

Claim 22. A process of forming a semiconductor structure according to claim 21, wherein the first thickness is less than the second thickness.

Claim 23. A semiconductor circuit comprising a substrate;

a plurality of field effect transistors formed on the substrate, the plurality of field effect transistors including a first portion of field effect transistors and a second position of field effect transistors;

a first stress layer having a first thickness and being configured to impart a first determined stress to the first portion of the plurality of field effect transistors; and

a second stress layer having a second thickness and being configured to impart a second determined stress to the second portion of the plurality of field effect transistors.

Claim 24. The semiconductor circuit according to claim 23, wherein:

the first portion of the plurality of field effect transistors have spacings between adjacent field effect transistors that fall within a first defined spacing range; and

the second portion of the plurality of field effect transistors have spacings between adjacent field effect transistors that fall within a second defined spacing range.

Claim 25. The semiconductor circuit according to claim 24, wherein:

the first defined spacing range is less than the second defined spacing range; and
the first thickness is less than the second thickness.